

cPCI 6150 Hot Swap Design Application Note

Features

The following are CompactPCI (cPCI) Hot Swap design (using the PCI 6150BB PCI-to-PCI Bridge device) reference design features. This 32-bit PCI-to-PCI Bridge device offers superior PCI performance, based on the PCI 6150 PCI-to-PCI Bridge device:

- *PCI Local Bus Specification, Revision 2.3 (PCI r2.3)*
- PCI buffer supports 3.3V signaling with 5V input signal tolerance and 1 KB buffering
- Asynchronous Frequency support for 33 and 66 MHz on primary Bus and 33, 40, 50, 60, or 66 MHz on secondary Bus
- *PICMG 2.1, R2.0, Hot Swap Specification (PICMG 2.1, R2.0)*, compliant with PI=1 support

General Description

The *performance-tuned* PCI 6150, a *PCI r2.3*-compliant, 32-bit PCI-to-PCI Bridge device, offers an excellent performance solution for various adapters and embedded systems.

The PCI 6150, 32-bit PCI-to-PCI Bridge device is designed for high-performance, high-availability applications in Hot Swap Bus expansions, programmable data transfer rate control, frequency conversions from slower to faster, or faster to slower, PCI Buses. The PCI 6150 offers sophisticated buffer management and configuration options designed to provide customizable performance optimization.

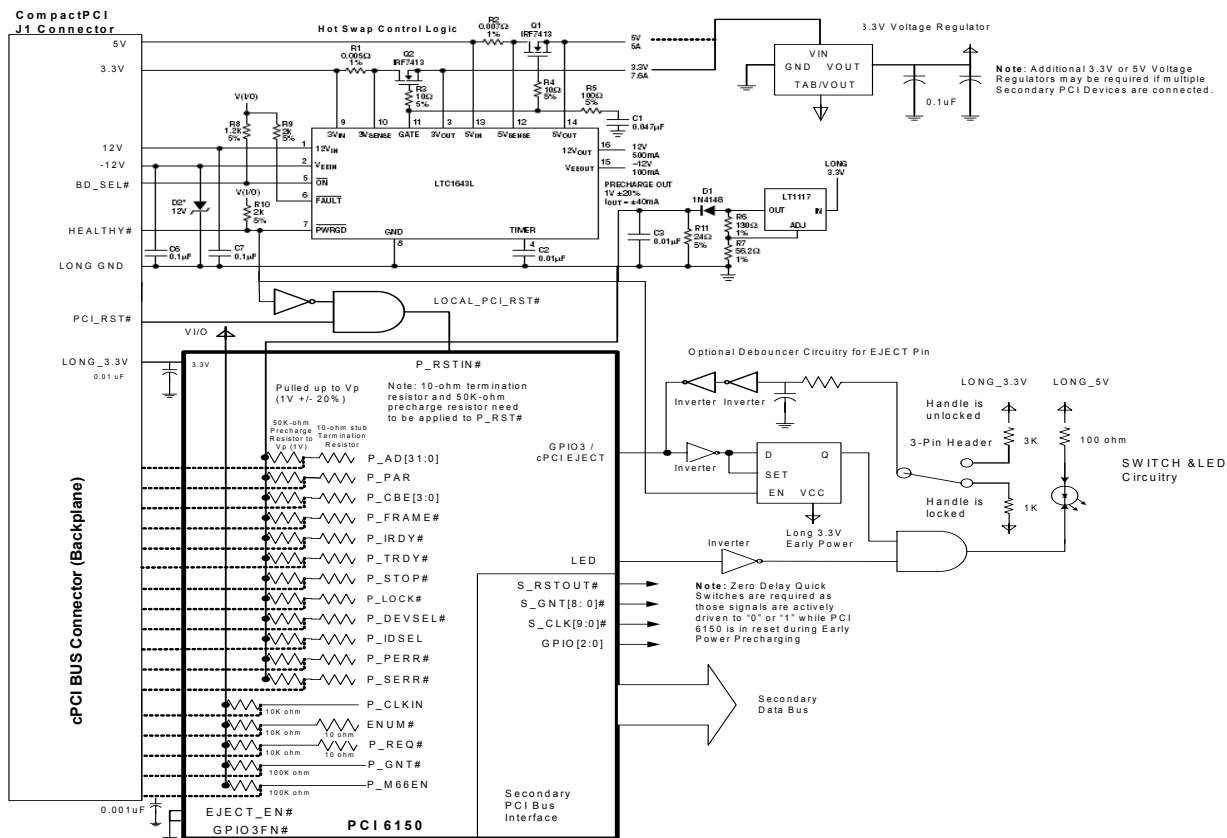


Figure 1. cPCI 6150 Hot Swap Design Block Diagram

Revision History

Date	Version	Comments
03/2004	1.0	Initial release.

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Introduction

This application note provides design information for a cPCI Hot Swap Add-In card, using the PCI 6150 PCI-to-PCI Bridge. The subsystem described in this application note consists of a cPCI 6150 Board and Hot Swap control logic.

The PCI 6150 is equipped with Hot Swap register support and the following Hot Swap Control pins—EJECT_EN# ENUM#, GPIO3FN#, and LED—which provide Hot Swap Design capability. The PCI 6150 incorporates Hot Swap functionality, which meets *PICMG 2.1, R2.0* requirements.

1 Architecture

1.1 Enabling PCI 6150 cPCI Hot Swap Feature

To enable the PCI 6150 cPCI Hot Swap Feature, connect EJECT_EN# and GPIO3FN# to 0. If the Hot Swap feature is not enabled, connect GPIO3 to Logic 0. ENUM# may remain unconnected.

1.2 PCI 6150 Hot Swap Control Signals

Table 1 describes the Hot Swap Control signals—EJECT_EN# (GPIO3), ENUM#, GPIO3FN#, and LED.

Table 1. Hot Swap Control Signals Description

Pin	Name	Description
EJECT_EN# (GPIO3)	Hot Swap Ejector Switch	EJECT_EN# (GPIO3) is multiplexed with the GPIO3 pin. To configure EJECT_EN# (GPIO3) as a Hot Swap EJECT_EN# pin, both EJECT_EN# and GPIO3FN# must be pulled down to 0. If the Hot Swap feature is not utilized, connect EJECT_EN# (GPIO3) to Logic 0. By pulling EJECT_EN# and GPIO3FN# low, the PCI 6150 enables GPIO3 to behave as the EJECT_EN# pin. The PCI 6150 is equipped with an internal de-bouncer for EJECT_EN# (GPIO3). It has a range of 7.5 to 15 ms of de-bouncing time when EJECT_EN# (GPIO3) is closed. It is recommended, however, that external de-bouncer logic be implemented to provide additional EJECT_EN# (GPIO3) de-bouncing when EJECT_EN# is closed during Insertion.
ENUM#	Enumerator Output Signal	Used to notify system host that a board has been freshly inserted or is about to be extracted. Asserted when the Hot Swap Control/Status register (Offset E6h) INS (Insertion State) or EXT (Extraction State) bit is set.
GPIO3FN#	GPIO3 Function Select	When GPIO3FN# is tied high, GPIO3 acts only as a GPIO pin, regardless of the EJECT_EN# pin state. GPIO3 acts as ejector input only when both GPIO3FN# and EJECT_EN# are tied low.
LED	Status Blue LED	Upon Insertion, hardware automatically turns ON the LED until the Hardware Connection process completes. Upon Extraction, the LED remains OFF until the Hot Swap software Device driver turns ON the LED by setting the Hot Swap Control/Status register (Offset E6h) LOO (LED Status) bit to indicate that Extraction is permitted.

1.3 cPCI Bus Isolation

To implement the cPCI feature, 10-Ohm Stub Termination Series resistors are required for the PCI Bus signals. The trace length must be within 0.6 inches (15.2 mm) from the connector to the resistors (stub). During Insertion, place the cPCI Bus in a high-impedance state until the cPCI board is fully powered and enabled for access by the PCI Bus in Configuration space.

The following pins must be terminated with 10-Ohm Stub Termination Series resistors—ENUM#, P_AD[31:0], P_CBE[3:0]#, P_DEVSEL#, P_FRAME#, P_IDSEL, P_IRDY#, P_LOCK#, P_PAR, P_PERR#, P_RSTIN#, P_SERR#, P_STOP#, and P_TRDY#.

P_REQ# may require a Series Termination resistor (the size of the resistor depends on the buffer output at the driving pin). In this design, a 10-Ohm resistor is applied to P_REQ#.

P_CLKIN and P_GNT# do not require Stub Termination resistors, per *PICMG 2.0, R3.0, CompactPCI Specification (PICMG 2.0, R3.0)*.

TCK, TDI, TDO, TMS, and TRST# do not require a Stub Termination resistor.

Power-On Reset

The PCI Bus Resets when RST# is active during power-on. The Hot Swap Control Logic inputs PCI_RST# from the cPCI Bus backplane and generates LOCAL_PCI_RST#. After LOCAL_PCI_RST# is driven active, LOCAL_PCI_RST# remains asserted throughout the Physical Connection process. As mandated in *PCI r2.3*, the PCI 6150 asynchronously three-states all primary PCI Bus signals and most secondary PCI Bus signals while LOCAL_PCI_RST# is asserted.

However, the secondary PCI Bus signals—GPIO[2:0], S_CLK[9:0], S_GNT[8:0]#, and S_RSTOUT#—are continuously driven to 1, 0, or 1/0 by the PCI 6150 when LOCAL_PCI_RST# is asserted. If these pins are driven while the PCI 6150 is in Reset, they may damage the PCI device I/O buffers connected to the secondary PCI Bus. To avert damaging the secondary PCI devices, it is recommended that Quick Switch Logics be applied to those secondary PCI pins previously mentioned on an as-needed basis, as those pins may not be directly interfaced to the secondary PCI device.

A series of Zero-Delay Quick switches are enabled to three-state these secondary PCI signals while Early Power is in process. After power is stabilized, the secondary PCI signals are able to switch the signal state to accommodate normal bus operation. To better illustrate the primary and secondary pin states during Reset, Table 2 delineates pin states when P_RSTIN# is actively driven.

Table 2. Pin States when P_RSTIN# is Actively Driven

Pins	P_RSTIN#=0	Pins	P_RSTIN#=0	Pins	P_RSTIN#=0
BPCC_EN	I	P_AD[31:0]	T	S_AD[31:0]	T
CFG66	I	P_CBE[3:0]#	T	S_CBE[3:0]#	T
EE_EN#	I	P_CLKIN	I	S_CFN#	I
EEPCLK	D1	P_DEVSEL#	T	S_CLKIN	I
EEPDATA	D1	P_FRAME#	T	S_CLKO[9:0]	D01
EJECT_EN#	I	P_GNT#	I	S_DEVSEL#	T
ENUM#	T	P_IDSEL	I	S_FRAME#	T
GPIO0	D1	P_IRDY#	T	S_GNT[8:0]#	D1
GPIO1	D0	P_LOCK#	T	S_IRDY#	T
GPIO2	D0	P_M66EN#	I	S_LOCK#	T
GPIO3FN#	I	P_PAR	T	S_M66EN#	I
MSK_IN	I	P_PERR#	T	S_PAR	T
OSCSEL#	I	P_REQ#	T	S_PERR#	T
OSCIN	I	P_SERR#	T	S_REQ[8:0]#	I
		P_STOP#	T	S_RSTOUT#	D0
		P_TRDY#	T	S_SERR#	T
				S_STOP#	T
				S_TRDY#	T

1.4 Hot Swap Control Logic

In this application, the LTC1643L-1 Hot Swap controller (designed by Linear Technology, for hot swapping cPCI boards) is used. The +3.3V, +5V, +12V, and -12V inputs to the LTC1643L are derived from medium-length Power pins. The LONG_3.3V, 5V and VIO pins are utilized to provide power to the pull-up resistors, Bus Pre-charge circuits, the PCI 6150 PCI-to-PCI Bridge device, and LOCAL_PCI_RESET# Logic circuitry. The cPCI backplane BD_SEL# signal is connected to the LTC1643L ON# pin and the LTC1643L PWRGD# pin is connected to the backplane HEALTHY# signal. The LTC1643L PWRGD# signal is combined with the PCI_RST# signal to generate LOCAL_PCI_RESET# to the PCI 6150.

The primary PCI Bus V_p (1V reference voltage) is generated using an LT1117 Low Dropout regulator. The LT1117 output is set to 1.8V, then the voltage is dropped by a 1N4148 diode to generate a 1V reference voltage. The V_p 1.0V ($\pm 20\%$) reference bias voltage is required to power the pre-charge circuits. When the system is ready for normal operation, the on-board pre-charge bias voltage source is required to bring the network to the required bias voltage.

For further data on required conditions for the selection of $V_{PSOURCE}$ and V_p and pre-charge resistor disconnection on the PCI 6150 primary PCI Bus signals during normal operation, refer to *PICMG 2.1, R2.0*, Sections 3.1.3.1 and 3.1.3.3.

1.5 Pre-Charge Circuitry Required for Primary PCI Signals

Most cPCI 6150 Hot Swap board primary PCI Bus signals require pre-charge circuitry when the pre-charge bias voltage is applied to the cPCI board through a high-impedance source during Hot Swap Insertion. During Early Power, pre-charging of the Long Power pins (3.3 and 5V), Medium pins (PCI Control signals and standard Power pins), and Short pin (BD_SEL#) is kept to less than 4 ms. To facilitate pre-charging during Hot Swap Insertion or Extraction, the signals delineated in Table 3 must be connected to specific voltage sources.

In this application, the V_p 50K- or 51K-Ohm pre-charge resistors, of the intended cPCI 6150 Hot Swap board, remain connected with an active V_p power source (1V). The PCI signal leakage remains within the tolerable high-level leakage current of L_{IH}

(+55 μ A) on the PCI Bus I/Os when the Backend power stabilizes, and the PCI Bus is ready for normal bus operation while BD_SEL# and HEALTHY# are actively asserted.

Note: The PCI 6150 is not capable of bus parking when the bus returns to idle.

Table 3. Signal Voltage Sources

Voltage	Pin
10K to VIO	P_CLKIN, ENUM#, P_REQ#, P_RSTIN# (HEALTHY# does not require pre-charging)
100K to VIO	P_GNT# and P_M66EN
50K or 51K to V_p (1V Reference Voltage)	P_AD[31:0], P_CBE[3:0]#, P_DEVSEL#, P_FRAME#, P_IDSEL, P_IRDY#, P_LOCK#, P_PAR, P_PERR#, P_RSTIN#, P_SERR#, P_STOP#, P_TRDY#

1.6 BD_SEL# State Engaged

BD_SEL# is the shortest Hot Swap Interface pin. It is the last to mate during Insertion and the first to disengage during Extraction. BD_SEL# is utilized for sensing whether its connection takes place at a time when all other primary PCI pins are reliably connected. It is driven low to enable the Backend Powering sequence, by way of the Hot Swap ON# Control signal. For a cPCI system not implementing the Hot Swap Control logic, BD_SEL# is grounded on the backplane. During Insertion, the Hot Swap controller controls Backend power ramping by asserting BD_SEL# to bring the state of Insertion from P1/H0 (Physical Connection State 1, transitioning to the Hardware Connection where the board is fully seated, but not powered, and not active on the PCI Bus) to H1 (Hardware Connection State 1, where the board has powered up and is sufficiently initialized to connect to the PCI Bus). When BD_SEL# mates with the backplane, the Physical Connection process is complete. BD_SEL# is continuously asserted until Backend power gradually disengages. When BD_SEL# detaches from the cPCI Backplane connector, the PCI 6150 immediately transitions to the H0 state (powered off) and the Software Device driver should be in the S0 state (Software Device driver enters a quiescent state).

1.7 HEALTHY# during Insertion and Extraction States

As mandated by *PICMG 2.1, R2.0*, the cPCI Hot Swap board facilitates HEALTHY#, which is driven active to indicate board readiness to be connected to the cPCI Bus. HEALTHY# is an Open Drain pin ($I_{OL} = 4 \text{ mA}$). During Insertion, HEALTHY# should not be actively driven if Backend power is not within the required tolerance ($\pm 5\%$, per *PICMG 2.1, R2.0*). After Backend power is stabilized, HEALTHY# is asserted, together with a prior assertion of BD_SEL#, to indicate that the H1 state is reached (board has powered up and is sufficiently initialized to connect to the PCI Bus).

In this cPCI 6150 Hot Swap application, the cPCI backplane HEALTHY# pin is connected to the Hot Swap controller PWRGD# signal. PCI_RST# and PWRGD# are connected through an AND Gate, by way of an inverter, to provide LOCAL_PCI_RST# signaling. When LOCAL_PCI_RST# is active, P_RSTIN# is actively driven to Reset the PCI 6150 and causes the PCI 6150 to three-state the output pins (in High Impedance mode) during pre-charge. During Extraction, HEALTHY# is de-asserted when the Power pins begin to disengage from the cPCI Bus connector.

1.8 Ejector Switch

The ejector switch is used to signal cPCI Hot Swap board Insertion or impending Extraction. During Insertion, the switch is closed, causing the INS bit to be set. ENUM# is then asserted to the system host to notify that a board has been freshly inserted or is about to be extracted. After the board is fully seated and the PCI 6150 is visible to the system with the LED turned OFF, the System Hot Swap software must clear the INS bit to clear the ENUM# signal. As a result, the EXT bit is set, indicating that Extraction is permitted.

During Extraction, the switch is open from a closed position, which sets the EXT bit to 1. When the Extraction bit is set to 1, ENUM# is asserted to the system host, indicating that the board is about to be extracted. After ENUM# is acknowledged by the system host for Extraction process, the System Hot Swap software must clear the EXT bit to clear the ENUM# signal. As a result, the INS bit is set, indicating that Insertion is permitted.

As previously mentioned, external de-bouncer logic is implemented on the EJECT_EN# pin to provide additional de-bouncing when the ejector switch is closed during Insertion.

1.9 LED Function

During Insertion, the PCI 6150 turns ON the LED when Reset is asserted and the LED remains ON until Reset is de-asserted. As a Hot Swap PI=1 Compliant device (with device hiding feature), although Reset is de-asserted, keep the LED ON until the ejector switch closes.

The PCI 6150 implements the LED as PI=0 time sequence (LED is turned OFF when Reset is de-asserted). Therefore, external circuitry is provided in the block diagram to ensure that the PCI 6150 is Hot Swap PI=1 compliant. (Refer to the LED external circuitry in Figure 1.) During the Extraction process, the LED remains OFF until it is turned ON by the Software Device driver, which sets the LOO bit to 1, indicating that the Software Device driver is quiescent and that Extraction is permitted.

1.10 Implementing Device Hiding

The PCI 6150 is equipped with a Device Hiding Control and Status bit—the Hot Swap Control/Status register (Offset E6h) DHA (Device Hiding Arm) bit—which determines whether device hiding is enabled. Device hiding allows a board that is software disconnected and authorized for Extraction to be invisible on the cPCI Bus, thereby avoiding jeopardy to the system if a PCI transaction is in progress when Extraction occurs. During Insertion, device hiding is enabled with the DHA bit set to 1, arming device hiding when LOCAL_PCI_RST# is de-asserted.

When the switch is closed, the INS bit is set to 1 and the Hot Swap Control register DHA bit is cleared from the PCI 6150, disarming device hiding. During Extraction, the PCI 6150 remains visible to the system host until the LED is ON with the LOO bit set to 1. When the ejector switch is open, the PCI 6150 goes into Device Hiding mode with the DHA bit set to 1.

1.11 Interrupt Routing

The PCI 6150 is not equipped with PCI Interrupt pins. Interrupt circuitry may be externally required. For further details, refer to the *Interrupt Binding Rule Application Note*, which may be obtained by contacting PLX Technical Support at www.plxtech.com/support/.

2 Assumptions

Board components for this design (*such as* boot and code memory, serial EEPROM, and pull-up/down resistors) are not discussed in this application note. Designers are expected to add these components, as needed.

3 References

The following is a list of documentation to provide further details.

- *PCI 6150 Data Book, Version 2.0*, May, 2003
PLX Technology, Inc.
870 Maude Ave., Sunnyvale, CA 94085 USA
Tel: 408-774-9060 or 800-759-3735, Fax: 408-774-2169, <http://www.plxtech.com>
- *PCI Local Bus Specification, Revision 2.3*
PCI Special Interest Group (PCI-SIG)
5440 SW Westgate Drive #217, Portland, OR 97221 USA
Tel: 503 291-2569, Fax: 503 297-1090, <http://www.pcisig.com/home>
- *LTC1643L/LTC1643L-1/LTC1643H, PCI-Bus Hot Swap Controller Data Sheet*,
Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417 USA
Tel: 408-432-1900, Fax: 408-434-0507, <http://www.linear.com>
- *PICMG 2.0, R3.0, CompactPCI Specification*, October 1, 1999
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c/o Virtual Inc., 401 Edgewater Place, Suite 500, Wakefield, MA 01880 USA
Tel: 781 246-9318, Fax: 781 224-1239, <http://www.picmg.org>
- *PICMG 2.1, R2.0, CompactPCI Hot Swap Specification*, January 2001
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